MR1957-332

CLEAN COPY OF AMENDED CLAIMS:

1. (Amended) A semiconductor packaging structure for packaging a semiconductor element comprising:

a flat substrate having a chip seat formed thereon and having a plurality of outer lead wires contiguous a top surface of said flat substrate and extending to a bottom surface of said flat substrate;

a1 a wall formed of a molding compound and positioned along a periphery of said flat substrate, said wall having a lateral wall thickness;

a liner positioned between said wall and said plurality of outer lead wires, said liner having a lateral liner thickness greater than said lateral wall thickness; and,

a plurality of bonding wires electrically connecting said semiconductor element to said plurality of outer lead wires.

2. (Amended) The semiconductor packaging structure as recited in Claim 1 wherein a transparent upper cover is mounted on said wall.

a1

3. (Amended) The semiconductor packaging structure as recited in Claim 1 wherein a potting resin is adhered to said semiconductor element.

5. (Amended) The semiconductor packaging structure as recited in Claim 2 wherein a mouth groove is formed on an inner side of said wall for receiving said transparent upper cover.

a2

4

~~6~~. (Amended) The semiconductor packaging structure as recited in Claim 1 wherein said liner is formed of an electrically insulating material.

MARKED UP COPY OF AMENDED CLAIMS:

1. (Amended) A semiconductor packaging structure for packaging a semiconductor element comprising:

a flat substrate having a chip seat formed thereon and having a plurality of outer lead wires contiguous a top surface of said flat substrate and extending [through lateral sides of the substrate] to [the] a bottom surface of [the] said flat substrate;

a wall formed [by] of a molding compound and [installed at] positioned along a periphery of [the] said flat substrate [so as to be formed as a groove on the flat substrate], said wall having a lateral wall thickness;

a liner [for supporting the wall, and the liner extending inwards and outwards than the wall with a predetermined distance to prevent that a mold flush problem will induce in the wall] positioned between said wall and said plurality of outer lead wires, said liner having a lateral liner thickness greater than said lateral wall thickness; and,

a plurality of bonding wires [on the elements for being electrically connected to the outer circuit] electrically connecting said semiconductor element to said plurality of outer lead wires.

2. (Amended) The semiconductor packaging structure as [claimed] recited in Claim 1[,] wherein a transparent upper cover [is installed on the element] is mounted on said wall.

3. (Amended) The semiconductor packaging structure as [claimed] recited in Claim 1[,] wherein a potting resin is [installed on the element] adhered to said semiconductor element.

5. (Amended) The semiconductor packaging structure as [claimed] recited in Claim [1,] 2 wherein a mouth groove is [installed at the] formed on an inner side of [the] said wall for [indicating the mounting of the] receiving said transparent upper cover.

6. (Amended) The semiconductor packaging structure as [claimed] recited in Claim 1[,] wherein [the material of the] said liner is formed of an electrically insulating [plant] material.